Performance Variation Adaptive Differential Signaling via Carbon-Nanotube Bundles

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Abstract

Carbon Nanotube (CNT) interconnects provide one of the most promising on-chip interconnect techniques for future VLSI systems, although significant process and runtime variabilities remain challenging for CNT interconnects. In this paper, we propose a performance variation adaptive differential signaling scheme, particularly for carbon nanotube bundle on-chip interconnects. Estimation based on published data demonstrate 37% signal propagation performance variation reduction achieved by the proposed scheme impplemented in CNT bundles compared with CNT interconnects with the conventional signaling scheme.

1 Introduction

Phenomenal nanotechnology research development have achieved fabrication of a variety of nanoscale devices, including nanowire and carbon nanotube transistors and molecular devices. These devices are promising to form the basic blocks of future VLSI systems.

Besides device manufacturing, system integration techniques are much needed for nanotechnology based VLSI systems. Global interconnects form the bottleneck of VLSI system performance. Current VLSI on-chip interconnect technology can hardly be scaled down into the nanometer domain, due to its conductivity and performance limitation. Alternative interconnect techniques must be developed for nanoscale VLSI systems.

Carbon nanotube technology provides a promising on-chip interconnect technique for future VLSI design. A single-walled carbon nanotube (SWCNT) is a one-atom-thick graphite sheets rolled up in a cylinder of a nanometer-order diameter. A carbon nanotube is either metallic or semiconductive, depending on its chirality (Fig. 1). If non-chiral, a SWCNT interconnect has a current density more than 1000X larger than a metal interconnect. These SWCNT interconnects naturally align themselves into bundles or ropes via Van der Waals forces, providing improved conductivity [3, 5, 9].

Increased variability is an inevitable growing challenge for nanoscale VLSI circuits as a result of process limitation and fundamentals of quantum physics. CNT bundle interconnects are subject to greater variabilities than copper interconnects, e.g., CNT bundle interconnects need to reduce their geometric variability by 63% to achieve the same amount of variability as copper interconnects [8]. Such variability leads to potential performance degradation and system malfunction. Robust design techniques must be developed for CNT interconnects.

Low-swing differential signaling is an effective technique which reduces power consumption and enhances noise immunity of VLSI on-chip interconnects [6, 10, 11, 12]. By employing a sense amplifier at the receiver’s end, a small amount of current suffices to trigger the receiver flip-flop, avoiding total capacitive charge of the interconnect. The differential structure ensures noise immunity by rejecting any common noise injected by neighboring interconnects or power/ground supply networks.

In this paper, I extend the differential signaling technique, and propose a performance variability adaptive signaling scheme for carbon nanotube bundles. In additional to a voltage reference signal which achieves common noise rejection in a differential structure, I include a performance reference signal, which has equal variation as the data signals under spatial correlation of process and runtime variations, thus avoiding timing violation for the receiver flip-flop. The pro-
posed scheme is particularly suited for CNT bundles, wherein 37% performance variation reduction is achieved compared with the conventional interconnect scheme.

The rest of the paper is organized as follows. Section 2 briefly introduces the challenge of global interconnection, CNT interconnects, and the related existing interconnect design techniques. Section 3 presents the proposed performance variation adaptive differential signaling scheme for CNT bundles. Section 4 gives numerical examples which estimate the resultant performance variation reduction, before we conclude in Section 5.

2 Background

2.1 Global Interconnect Challenge

VLSI technology scaling achieves high performance and low power by reduced capacitive load for a device. However, as Rent’s rule dictates, length distribution of VLSI interconnects follows a power law [4]. A small number of global interconnects form bottleneck for VLSI performance.

Current VLSI technology scaling trend brings increasingly significant interconnect resistance and capacitance (due to skin effect and lateral coupling capacitance), and degraded interconnect performance and signal integrity. For on-chip interconnects in nanoscale VLSI systems, new circuit design and manufacturing techniques must be developed.

2.2 CNT Interconnects

CNT interconnects emerge as the most promising solution for future VLSI system on-chip interconnection, due to their outstanding electronic, thermal, and mechanical properties. A metallic CNT has the mean free path of electrons on the order of micrometers compared with few tens of nanometers in copper interconnects [5], and a current density on the order of $10^9$ A/cm$^2$ [9]. Their sp2 carbon bonds are even stronger than the sp3 bonds in diamonds, making CNTs mechanically strong [3].

Technology scaling leads to inevitable increase of process and system runtime variations due to limitations of process technology and even the fundamentals of quantum physics. Under current manufacturing technology, process variations in CNT interconnects are much larger than in copper interconnects. Metallic CNT occurrence probability, CNT geometry, contact resistance, electron mean free path, and intra-bundle dielectric thickness are subject to up to 50% variation. These variations lead to significant performance and power consumption variabilities in CNT interconnects. In order to achieve the same percentage of variation in both CNT bundles and copper interconnects, the percentage variation in CNT bundle dimensions must be reduced by 63% in 22nm technology [8].

Before significant improvement is achieved in nanotechnology for process stability, circuit and layout design techniques have to be developed to achieve high performance, low power, and robust on-chip interconnects for nanotechnology based VLSI systems.

2.3 Related Design Techniques

An example of circuit design technique for robustness against variability is a timing error tolerant flip-flop, which includes a shadow latch sampling the input data at a deferred time (e.g., at the clock falling edge while the main latch samples the input data at the clock rising edge). Mismatch of the sampled data by the main latch and the shadow latch indicates a timing error, and triggers a data recover procedure which overwrites the sampled data in the shadow latch into the main latch [1].

An outstanding interconnect design challenge comes from large capacitive loads of long interconnects. Charging large capacitive loads compromises signal propagation performance, signal integrity, and power consumption. Low swing interconnects are effective in avoiding fully charging of the large capacitive load, by propagating and detecting signals of reduced swing at the receiver’s end by sense amplifiers. Low swing interconnects achieve reduced power consumption and improved signal propagation performance [11, 12].

For noise immunity, differential signaling is often combined with low swing signaling. In such a scheme, a pair of identical interconnects are routed parallel in close proximity. A differential sense amplifier at the receiver’s end amplifies the differential signal, and rejects any common noise injected on the interconnect pair, achieving enhanced noise immunity [6, 10].

For improved noise immunity, the differential sense amplifiers at the receiver’s end are often implemented in current-sensing circuits, which are insensitive to noise induced voltage offset on the interconnects [6]. Fig. 2 presents a typical current-sensing based differential low swing interconnect implementation.
3 Performance Variability Adaptive Differential Signaling

3.1 Timing Requirements

First, let us recall the timing requirements, e.g., the setup and the hold time constraints in a synchronous VLSI design as follow.

\[
\begin{align*}
D_{\text{clk}} - Q + D_{\text{data}} & \leq T_{\text{cycle}} - T_{\text{setup}} + D_{\text{skew}} \\
D_{\text{clk}} - Q + D_{\text{data}} & \geq T_{\text{hold}} + D_{\text{skew}}
\end{align*}
\]

(1)

where \(D_{\text{clk}} - Q\) is the clock pin to the \(Q\) pin delay within a flop-flop, \(D_{\text{data}}\) is the signal propagation delay along a data path, \(T_{\text{cycle}}, T_{\text{setup}},\) and \(T_{\text{hold}}\) are cycle time, setup time, and hold time, respectively, and \(D_{\text{skew}}\) is the clock skew, i.e., the clock arrival time at the receiver flop-flop minus the clock arrival time at the launch flop-flop.

3.2 Performance Variation Adaptive Signaling

For timing variation adaptive design, I propose to route a clock path in parallel with a data path, such that the clock skew is given by the clock propagation delay from the launch flip-flop to the receiver flip-flop, equal to the data path delay. The clock path is routed in close physical proximity to the data path, such that they are fully correlated. In timing constraints, any data path delay variation is accompanied with an equal clock skew variation, which cancel each other, and lead to no timing violation (Fig. 3).

\[
\begin{align*}
D_{\text{clk}} - Q + D_{\text{data}} + \epsilon_{\text{data}} & \leq T_{\text{cycle}} - T_{\text{setup}} + D_{\text{skew}} + \epsilon_{\text{skew}} \\
D_{\text{clk}} - Q + D_{\text{data}} + \epsilon_{\text{data}} & \geq T_{\text{hold}} + D_{\text{skew}} + \epsilon_{\text{skew}} \\
D_{\text{data}} & \approx D_{\text{skew}} \\
\epsilon_{\text{data}} & \approx \epsilon_{\text{skew}}
\end{align*}
\]

(2)

The clock skew which is equal to the data path delay is a useful clock skew, which helps to locate the nominal clock skew at the center of a permissible timing window.

\[
T_{\text{hold}} \leq D_{\text{clk}} - Q + D_{\text{data}} - D_{\text{skew}} \leq T_{\text{cycle}} - T_{\text{setup}}
\]

(3)

3.3 Performance Variation Adaptive Differential Signaling

The above-mentioned performance variation adaptive signaling scheme can be extended by combining with differential signaling (Fig. 4). The data and the clock signals are respectively shielded by a ground signal against coupling noise. The differential receivers improve signal robustness by rejecting common noise among the data-ground and the clock-ground signal pairs. The current-mode differential signaling scheme is insensitive to voltage variation due to injected noise, and the close current loop formed by the differential pair minimizes noise injection to other interconnects.

3.4 CNT Bundle Implementation

The proposed performance variation adaptive (differential) signaling is best fitted in a CNT bundle implementation. The abundant CNTs in a bundle facilitate parallel routing of the data, the clock, and the ground signals. The intra-bundle parametric variations are much smaller than the inter-bundle parametric variations, which leads to significant performance variation reduction, as is shown in the next section.

4 Numerical Example

Let us compare performance variation of CNT bundles in the proposed timing variability adaptive signaling scheme and CNT bundles in the conventional signal scheme in this section. The proposed nanotube bundle signaling effectively moves data and clock signal in the same nanotube bundle, such that the data and the clock signals differ in signal propagation performance only because of intra-bundle variations, and are immune to inter-bundle variations. Let us follow the analysis in [8], and study nanotube bundle signal propagation performance variation due to 10 parametric variations. The 3\(\sigma\) variations of the parametric variations and the 3\(\sigma\) variations of their impact on signal propagation performance are shown in Table 1.
The global CNT bundles are 1mm long, 22nm wide and 22nm high. Within the bundle are 400 nanotubes of 0.8nm diameter, and 0.34nm spacing. Table 1 gives the inter-bundle variations as the average of a nanotube bundle, and the intra-bundle variations for each individual nanotube. Note that the relative deviation $\sigma/\mu$ of a collection of $n$ independent identical variations is given as follows.

$$\frac{\sigma(\sum X_i)}{\mu(\sum X_i)} = \frac{\sigma(X)}{\sqrt{n} \mu(X)} \quad (4)$$

For CNT bundles in the conventional signaling scheme, the collective effect of parametric variations are captured by the standard deviation of sum of independent variations as follows.

$$\sigma^2(\sum x_i) = \sum \sigma^2(x_i) \quad (5)$$

which gives a $3\sigma = 50.03\%$ inter-bundle delay variation (among which 12.55% is contributed by the 1/3 probability for a CNT to be metallic) [8].

For the proposed performance adaptive signaling scheme, we propose to form a CNT bundle which includes data and clock links (and the ground signal in a differential signaling scheme), e.g., 400 CNTs for data link and 400 CNTs for clock link (and 400 ground signal in a differential signaling scheme). This gives the deviation between the data and the clock links as $3\sigma = 12.80\%$, among which 12.55% is solely contributed by the 1/3 probability for a CNT to be metallic.

Going from the conventional signaling scheme to the proposed performance variation adaptive (differential) signaling scheme achieves an estimate of 37.23% decrease of performance variation along a CNT bundle. The majority of the remaining performance variation is solely due to the metallic CNT occurrence probability, which depends on the chirality of a CNT. Any manufacturing technique which could control the chirality of a CNT would dramatically reduces CNT performance variation.

### 5 Conclusion

Process variation induced conductivity and signal propagation performance variation are outstanding challenges for carbon nanotube interconnects. In this paper, I propose performance variability adaptive differential signaling for carbon nanotube bundle based interconnects. I propose to include a performance reference signal on the basis of a ground voltage reference signal in a differential signaling scheme, to be adaptive to the significant signal propagation performance variation in carbon nanotube interconnects. The numerical example based on published data demonstrates 37% signal propagation performance variation reduction achieved by the proposed signaling scheme compared with the conventional signal scheme implemented in carbon nanotube interconnects.

### References


