SSTA-SI: Statistical Static Timing Analysis in the Presence of Signal Integrity Effects

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Abstract—Signal integrity effects have significant impacts on VLSI performance variation and must be taken into account in statistical timing analysis. We study signal propagation delay variation induced by crosstalk aggressor signal in this paper. We establish a functional relationship between signal propagation delay and crosstalk aggressor signal alignment by deterministic circuit simulation, and derive closed form formulas for statistical distributions of output signal arrival times. Our proposed method can be smoothly integrated into a static timing analyzer, which runtime is dominated by sampling deterministic delay calculation, while probabilistic computation and updating take constant time. Our experimental results based on 1000μm global interconnect structures in BPTM 70nm technology and industry designs in 130nm technology show that lack of statistical crosstalk aggressor signal alignment consideration could lead to up to 114.65% (71.26%) differences in interconnect delay means (standard deviations), and 159.4% (147.4%) differences in gate delay means (standard deviations), while our method gives within 1.28% (3.38%) mismatch in interconnect output signal arrival time means (standard deviations), and within 2.57% (3.86%) mismatch in gate output signal arrival time means (standard deviations), respectively.

Index Terms—Design, reliability, verification.

I. INTRODUCTION

VLSI designs experience an increase of system performance variation due to increased manufacturing and system runtime variabilities, including lithographic, chemical-mechanical planarization (CMP) process related, and dopant variations during manufacturing process, and supply voltage and temperature variations during system runtime. Consequently, VLSI performance verification moves away from the traditional over-pessimistic case analysis and explicitly addresses this increased variability. Statistical static timing analysis (SSTA) computes signal arrival time distributions at each pin (in block-based SSTA [1], [23]) or along each path (in path-based SSTA [15], [16]), and provides “timing yields” or probabilities for a chip to meet its timing requirements.

Statistical timing analysis accuracy has been significantly improved by including more variation sources into account. For example, a gate delay undergoes significant deviation when multiple inputs of the gate are switching at the same time. Neglecting this multiple-input switching effect could underestimate the mean delay of a gate by up to 20% and overestimate the standard deviation of a gate delay by up to 26% [2].

In this paper, we propose statistical timing analysis in the presence of signal integrity effects, by taking into account an equally significant source of variation in SSTA, i.e., the effect of crosstalk aggressor signal alignment on signal propagation delay of a victim interconnect and its driver gate. A crosstalk aggressor signal transition injects a noise into a victim net, and causes (1) interconnect delay variation [6], and (2) driver gate delay variation [20]. Such signal integrity effects have been taken into consideration in traditional deterministic timing analysis, and they must also be taken into consideration in statistical timing analysis. Existing publications address this effect based on the traditional “timing window” concept, which is oversimplified and inadequate [10], [19]. Our present work is the first in proposing an analytical statistical delay calculation method which takes signal integrity effects into account.

We organize the rest of this paper as follows. We present statistical timing analysis in the presence of signal integrity in Section II. We discuss runtime complexity, efficiency improvement techniques and other implementation issues in Section III. We present our experimental results in Section IV, before we conclude in Section V.

II. THEORY

A. Problem Formulation

Several signal integrity effects have significant impacts on signal propagation delay in a nanometer-scale VLSI design.
In this paper, we take into account the effect of crosstalk aggressor signal alignment on interconnect and gate delays in statistical timing analysis, and consider the following problem.

**Problem 1** [Statistical Delay Calculation in the Presence of Signal Integrity Effects]

Given

1. a system of coupled interconnects with their driver gates,
2. statistical signal arrival time variations at the inputs of the driver gates, and
3. statistical process parameter variations for the interconnects and their driver gates,

find statistical signal arrival time variations at the output of the system.

We list some of the notations that we use in this paper as follow.

- \( x_1(x_2) \) = input signal arrival time
- \( x' = x_2 - x_1 \) = crosstalk aggressor signal alignment
- \( D_g \) = driver gate delay
- \( y_1 \) = output signal arrival time
- \( \mu_1(\mu_2) = \mu_{x_1}(\mu_{x_2}) \) = mean of input signal arrival time
- \( \sigma_1(\sigma_2) = \sigma_{x_1}(\sigma_{x_2}) \) = standard deviation of input signal arrival time
- \( \text{cov}(x_1, x_2) \) = covariance of inputs signal arrival times
- \( \mu' (\sigma') = \mu_{x'}(\sigma_{x'}) \) = mean (standard deviation) of crosstalk aggressor signal alignment
- \( P(x) \) = probability density function (pdf) of \( x \)
- \( N(\mu, 3\sigma) \) = normal distribution of mean \( \mu \) and standard deviation \( \sigma \)

Algorithm 1 gives our proposed statistical timing analysis in the presence of signal integrity effects. We present the details of each step as follows.

**Algorithm 1: Signal Integrity Aware Statistical Timing Analysis**

**Input:** Coupled interconnects in R(L)/C networks, input signal arrival time distributions, other manufacturing/runtime variations

**Output:** Output signal arrival time distributions

1. Process variation extraction
2. Performance characterization
3. Probabilistic symbolic analysis
4. Statistical delay symbolic analysis in the presence of signal integrity effects

**B. Process Variation Extraction**

A signal arrival time in a nanometer-scale VLSI designs is affected by a number of correlated variational parameters, including inter-die, intra-die (location dependent), and purely random variations [13]. Such parameter variabilities can be extracted from a manufacturing process, and reduced to a minimum set of uncorrelated standard Gaussian random variables by applying principle component analysis (PCA) [4], [13], [21]. A signal arrival time \( x \) in a nanometer VLSI design can then be approximated in a polynomial function of such random variables [7], as follows.

\[
    x = f_1(r_1, r_2, \ldots) = \frac{1}{\sqrt{2\pi\sigma_r}} e^{-\frac{(r_1 - \mu_r)^2}{2\sigma^2_r}} \tag{1}
\]

**C. Performance Characterization**

To enable statistical propagation of signal arrival times across a coupled interconnect and its driver gate, we establish a functional relationship between an interconnect (its driver gate) delay and a crosstalk aggressor signal alignment. This is achieved by performing deterministic delay calculation for a set of “sampled” crosstalk aggressor signal alignments, and extract a (piecewise polynomial) function based on the sampling data. Such a characterization method is common, e.g., in analog design analysis and optimization which is known as the “training” process to establish functional relationships among variables [22]. We apply SPICE simulation for the most accurate delay calculation results, while interconnect model order reduction [14] and voltage controlled current source based gate modeling [5] techniques can be applied for efficiency improvement without significant accuracy loss.

Fig. 2 shows an interconnect delay as a function of crosstalk aggressor signal alignment for a pair of 1000nm coupled global interconnects in BPTM 70nm technology, for 10ps, 20ps, 50ps and 100ps input signal transition times, respectively.

![Fig. 2. Interconnect delay as a function of crosstalk aggressor signal alignment for a pair of 1000nm coupled global interconnects in BPTM 70nm technology, for 10ps, 20ps, 50ps and 100ps input signal transition times, respectively.](image-url)
We apply (least-mean-square) regression and approximate the victim net interconnect (driver gate) delay as a piecewise quadratic function as follows (where \(d_1 = d_2\) for interconnect delay).

\[
D_g = \begin{cases} 
  d_2 & x' \leq t_0 \\
  a_0 + a_1 x' + a_2 x'^2 & t_0 \leq x' \leq t_1 \\
  b_0 + b_1 x' + b_2 x'^2 & t_1 \leq x' \leq t_2 \\
  c_0 + c_1 x' + c_2 x'^2 & t_2 \leq x' \leq t_3 
\end{cases}
\]  

(2)

**D. Probabilistic Symbolic Analysis**

Traditional statistical timing analysis approaches compute moments (e.g., means, standard deviations, skewnesses, etc.) and correlations of signal arrival times in a design. It is critical to include correlations in these statistical timing analysis approaches to achieve meaningful and accurate estimation results. However, complexity arises in addressing an increasingly large degree of correlations. E.g., for \(n\) random variables, \(O(n^2)\) first-order correlations, and much more higher-order correlations are needed to compute exact probabilities. Truncating higher-order correlations gives accuracy-efficiency tradeoff.

Alternative to moments and correlation computation, signal arrival times in a design can be computed symbolically, e.g., in closed form expressions of variational parameters, such that their probabilistic distributions are accessible by, e.g., Monte Carlo simulation without the need of correlation computation. Such techniques include polynomial computation [7], affine arithmetics [12], probabilistic interval analysis [18], etc., where variational delays are computed by either derivation of closed-form formulas [12], [18], or by sampling analysis and regression [7], [8], [9]. We call these methods probabilistic symbolic analysis approaches.

We present closed-form formulas for statistical signal arrival time computation which takes constant time for improved efficiency compared with Monte Carlo simulation in the next section.

**E. Statistical Delay Calculation in the Presence of Signal Integrity Effects**

Given input arrival timing variations in closed form formulas of random variables and the functional relationship between the output and the input signal arrival times, we rewrite Problem 1 as follows.

**Problem 2** [Probability Density Function Propagation]

Given

1) joint probability density function of \(k\) random variables 

\(\vec{x} = <x_1, ..., x_k>\), and 

2) a piece-wise polynomial function \(y_1 = f(\vec{x})\), find probability density function of \(y_1\).

The output \(y_1\) stands for the signal arrival time distribution at one of the outputs of the coupled interconnect system. The random variables \(\vec{x}\) include variational process parameters, e.g., gate length and threshold voltage for the driver gates and interconnect widths and spacings for the load interconnects, and previous stage variations which give input signal arrival time variations. The piece-wise polynomial function combines process variation extraction and performance characterization results.

We partition the variable space of the function \(y_1 = f(\vec{x})\) into regions \(R_i \in \mathcal{R}\), within each region the output \(y_1\) has a consistent polynomial representation \(f_{R_i}\). We compute conditional probabilities for the output \(y_1\) for each region as follows.

\[
P(y_1 = \tau) = \sum_{R_i \in \mathcal{R}} \int_{\vec{x} \in R_i} P(\vec{x} \mid y_1 = \tau) d\vec{x}
\]

\[
= \sum_{R_i \in \mathcal{R}} \int_{\vec{x} \in R_i} P(x_1) \cdot P(x_2 \mid x_1)...
\]

\[
P(x_k = f_{R_i}^{-1}(y_1 = \tau, x_1, x_2, ..., x_{k-1})) dx_1 dx_2 ... dx_{k-1}
\]

(3)

For each \(y_1 = \tau\), its occurrence probability is given by the joint probability density function \(P(\vec{x})\) of \(\vec{x}\) to satisfy \(y_1 = f(\vec{x}) = \tau\). To guarantee \(y_1 = \tau\), we perform integration on \(k - 1\) dimensions, while the last variable \(x_k\) is given by the inverse function \(x_k = f^{-1}(y_1, x_1, x_2, ..., x_{k-1})\). Such an analytical inverse function \(x_k\) is available for any order-\(d\) polynomial approximation, where \(d \leq 4\).

For example [8], [9], consider a piece-wise quadratic approximation (2) of an output signal arrival time of two coupled interconnects, the probability density function of the output signal arrival time is given by:

\[
P(y_1) = \int_{-\infty}^{\infty} P(x_1 = y_1 - D_g) P(D_g) dD_g
\]

\[
= \int_{t_0}^{t_1} P(x_1 = y_1 - a_0 - a_1 x') P(x' \mid x_1) dx'
\]

\[
+ \int_{t_1}^{t_2} P(x_1 = y_1 - b_0 - b_1 x') P(x' \mid x_1) dx'
\]

\[
+ \int_{t_2}^{t_3} P(x_1 = y_1 - c_0 - c_1 x') P(x' \mid x_1) dx'
\]

\[
+ \int_{t_3}^{\infty} P(x_1 = y_1 - d_0) P(x' \mid x_1 = y_1 - d_0) dx'
\]

\[
+ P(x_1 = y_1 - d_1) (1 - \int_{t_0}^{t_3} P(x' \mid x_1 = y_1 - d_1) dx')
\]

\[
+ P(x_1 = y_1 - d_2) \int_{t_0}^{t_0} P(x' \mid x_1 = y_1 - d_2) dx'
\]

(4)

For the input signal arrival times in uncorrelated Gaussian distributions (i.e., in linear representation of uncorrelated Gaussian random variables), the crosstalk aggressor signal alignment \(x' = x_2 - x_1\) is also in a Gaussian distribution.

\[
P(x_1) = \frac{1}{\sqrt{2\pi}\sigma_1} e^{-\frac{(x_1 - \mu_1)^2}{2\sigma_1^2}}
\]

\[
P(x_2) = \frac{1}{\sqrt{2\pi}\sigma_2} e^{-\frac{(x_2 - \mu_2)^2}{2\sigma_2^2}}
\]

\[
P(x') = \frac{1}{\sqrt{2\pi}\sigma'} e^{-\frac{(x' - \mu')^2}{2\sigma'^2}}
\]

(5)
where
\[ \mu' = \mu_2 - \mu_1 \]
\[ \sigma'^2 = \sigma_2^2 + \sigma_1^2 + 2\text{cov}(x_1, x_2) \]

The conditional probabilities of the input signal alignment \( x' \) for each input signal arrival time \( x_1 \) have different means but the same variance.
\[ \mu_{x'|x_1} = \mu_{x_2} - x_1 \]
\[ \sigma'_{x'|x_1} = \sigma'_{x'} \]

Substituting the probability density functions \( P(x_1) \) and \( P(x' | x_1) \) in (5) to (4) gives
\[
P(y_1) = \frac{1}{\sqrt{2\pi\sigma_{ya}}} e^{-\frac{(y_1 - \mu_{ya})^2}{2\sigma_{ya}^2}} \frac{1}{2} (F(y_1, t_1, a_0, a_1, \sigma_{ya}) - F(y_1, t_0, a_0, a_1, \sigma_{ya}))
+ \frac{1}{\sqrt{2\pi\sigma_{yb}}} e^{-\frac{(y_1 - \mu_{yb})^2}{2\sigma_{yb}^2}} \frac{1}{2} (F(y_1, t_3, b_0, b_1, \sigma_{yb}) - F(y_1, t_2, b_0, b_1, \sigma_{yb}))
+ \frac{1}{2} P(x_1 = y_1 - d_0) (erf(\frac{t_2 - \mu_2 + y_1 - d_0}{\sqrt{2}\sigma'}) - erf(\frac{t_1 - \mu_2 + y_1 - d_0}{\sqrt{2}\sigma'}))
+ \frac{1}{2} P(x_1 = y_1 - d_1) (2 - erf(\frac{t_3 - \mu_2 + y_1 - d_1}{\sqrt{2}\sigma'}))
+ \frac{1}{2} P(x_1 = y_1 - d_2) (erf(\frac{t_0 - \mu_2 + y_1 - d_2}{\sqrt{2}\sigma'})) \tag{6}
\]

where
\[
F(y, t, k_0, k_1, \sigma_{yk}) = \text{erf} \left( \frac{1}{\sqrt{2\sigma'\sigma_{yk}}} (t\sigma_{yk}^2)
- \left( 1 - k_1 \right) (k_0 + \mu_2 - y)\sigma_1^2 + k_1 (k_0 + \mu_1 - y)\sigma_1^2 \right)
\]
\[
\mu_{ya} = \mu_1 + a_0 - a_1(\mu_2 - \mu_1)
\]
\[
\sigma_{ya} = \sqrt{(1 - a_1)^2\sigma_1^2 + a_1^2\sigma'^2}
\]
\[
\mu_{yb} = \mu_2 + b_0 - b_1(\mu_1 - \mu_2)
\]
\[
\sigma_{yb} = \sqrt{(1 - b_1)^2\sigma_1^2 + a_1^2\sigma'^2}
\]

Given process variation extraction results, the overall run-time is dominated by the number of crosstalk alignment configurations in performance characterization, which is given by \( N = O(\prod_{i=0}^{n} m_i) \) (\( N = O(\sum_{i=0}^{n} m_i) \)) for \( n \) crosstalk aggressors, each with \( m_i \) sampling alignments, when additivity cannot (can) be applied. For each crosstalk aggressor, the number of sampling alignments \( m_i = \text{MIN}(t_3 - t_0, 6\sigma')/l \) is given by the smaller of (1) \( t_3 - t_0 \) the time frame within which an aggressor signal transition makes a difference on the victim net driver gate delay, and (2) the \( 6\sigma' \)'s of the crosstalk alignment (which can be based on the input signal “timing windows”), for a given time step \( l \) between sampling crosstalk alignments.

We achieve improved efficiency by applying PCA to reduce the random variables to a minimum set of uncorrelated random variables. Having uncorrelated random variables significantly simplifies statistical computation. Of uncorrelated random variables \( \tilde{x} \), the joint probability density function is given by the product of each individual random variable’s probability density function \( P(\tilde{x}) = \prod_i P(x_i) \), and the sum of uncorrelated random variables \( \tilde{x} \) has its mean and variance given by
\[
\mu_{\sum_i x_i} = \sum_i \mu_i \quad \text{and} \quad \sigma^2_{\sum_i x_i} = \sum_i \sigma^2_i \]

We also improve efficiency by applying superposition for the effects of different variation sources on interconnect delay variation, due to the linearity of an R(L)C interconnect. For gate delay variations to which superposition finds limited application, we can leverage with the existing characterization and data mining techniques, e.g., adaptive regression which prioritizes the sampling space [11].

Our proposed statistical delay calculation in the presence of signal integrity effects can be implemented in a statistical timing analyzer, which goes through an iteration of pessimism reduction and estimation refinement, as is in traditional deterministic static timing analysis in the presence of signal integrity effects. An pessimistic distribution can be assumed initially and refined later during iteration.

### IV. Experiments

We apply our method to a variety of input signal transition times ranging from 10ps, 20ps, 50ps to 100ps and input signal alignment ranging from 50, 100, to 200ps. To cover different technology nodes, our test cases include 16X inverter which drive (I) a pair of 1000μm coupled global interconnects in 70nm technology given by BPTM, and (II) a pair of coupled interconnects which are extracted from a 130nm industry design with 451 resistors and 1637 ground and coupling capacitors.

We sample crosstalk aggressor signal alignment for every 2ps and apply SPICE simulation for the functional relationship between interconnect (gate) delay and crosstalk aggressor signal alignment. The results (Fig. 2 and similar figures for gate delay) verify the accuracy of our proposed piecewise-quadratic approximation.

We compare our proposed SSTA-SI with 1000 SPICE Monte Carlo simulation runs for interconnect (driver gate) delay and output signal arrival time variations. We include crosstalk aggressor signal alignment variation in a Gaussian...
distribution of 10\(\text{ps}\), 50\(\text{ps}\), 100\(\text{ps}\) or 200\(\text{ps}\) standard deviation and \(-10\text{ps}\), 0\(\text{ps}\), or 10\(\text{ps}\) mean. We bring into account the effects of manufacturing process variations on interconnect and gate delay variations, such effects differ with different crosstalk aggressor signal alignments. As an example, we assume a 100\% width correlation among local wire segments [17], and compute interconnect capacitances and resistances using closed form formulas [3] for normally distributed wire widths in SPICE Monte Carlo simulation. We consider a gate length variation in a normal distribution of which 3\(\sigma\) is 15\% of the minimum gate length [2].

We compare with statistical driver gate delay calculation without statistical crosstalk consideration, in which case one of the best practice is to assume a unit Miller factor by grounding all coupling capacitors. We observe that without statistical crosstalk consideration assuming a unit Miller factor results in up to 159.4\% (114.65\%) mismatch in mean driver gate delay, and up to 147.4\% (71.26\%) underestimate in standard deviation of driver gate (interconnect) delay in this case [8], [9].

We also observe that over a variety of technology nodes, input signal transition times and arrival time deviations, our method gives the means and the standard deviations of gate (interconnect) output signal arrival times within 2.57\% (2.00\%) and 3.86\% (3.38\%) of SPICE Monte Carlo simulation results, respectively [8], [9].

V. CONCLUSION

We propose SSTA-SI: statistical static timing analysis in the presence of signal integrity effects. We study interconnect and gate delay variations induced by crosstalk aggressor signal alignment, i.e., signal arrival time difference at a coupled neighboring interconnect. This is a significant source of variation, which must be taken into consideration in statistical timing analysis. We present closed-form formulas for probabilistic gate delay calculation based on deterministic delay calculation for sampling crosstalk alignment configurations. After sampling delay calculation, probabilistic delay calculation and updating take constant time. Our experimental results based on 100\(\mu\)m global interconnect structures in BPTM 70\(\text{nm}\) technology and industry designs in 130\(\text{nm}\) technology verifies our method, which achieves within 1.28\% (3.38\%) mismatch for interconnect output signal arrival time means (standard variations), and within 2.57\% (3.86\%) mismatch for gate output signal arrival time means (standard variations) compared with SPICE Monte Carlo simulation results, while lack of statistical crosstalk alignment consideration could lead to up to 114.65\% (71.26\%) differences in interconnect delay means (standard deviations), and up to 159.4\% (147.4\%) differences in gate delay means (standard variations), respectively.

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