Defect Mapping and Adaptive Configuration of Nanoelectronic Circuits Based on a CNT Crossbar Nano-Architecture

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Abstract—Successful fabrication of a variety of nanoscale devices leads to research on nanoscale device integration, nano-architecture exploration, and nanoelectronic design techniques. This paper proposes a complete set of linear complexity catastrophic defect mapping techniques for CNT crossbar nano-architecture, as well as an adaptive CNT matching method for double gate CNFETs in the presence of CNT misalignment. Combined with adaptive nano-addressing method, these proposed techniques enable adaptive configuration of nanoelectronic circuits of correct functionality, performance, and reliability based on the CNT crossbar nano-architecture.

I. INTRODUCTION

As ITRS predicts, silicon based VLSI technology scaling, which has driving the semiconductor industry in the past five decades, is rapidly approaching its end. Fortunately, nanotechnology has achieved significant progress in recent years, leading to successful fabrication of a variety of nanometer scale devices, e.g., molecular diodes [19] and carbon nanotube field effect transistors (CNFETs) [20]. This provides new opportunities for VLSI technology to continue scaling in a post-silicon-based-technology era, and motivates active research on nanoscale device integration and nano-architecture design for next generation of non-silicon based nanoelectronic systems.

The early nanoelectronic architecture NanoFabrics was based on now obsolete devices of molecular resonant tunneling diodes (RTDs) and negative differential resistors (NDRs) [9]. The majority of the existing nanoelectronic architectures are based on a hybrid nano-CMOS technology [4], [6], [8], [15], [17], [21], [22], [24], wherein CMOS circuits are employed to realize the entire logic functions [21], [22], or complement nanoscale diode logic arrays by providing precharge and evaluation transistors and form sequential elements [4], [6], or form the periphery circuits for nanoscale memories [15], [24], [8]. This leads to compromised scaling advantages. The third category of existing nanoelectronic architectures rely on DNA-guided self-assembly to form 2-D scuffles for nanotubes [14], [18]

or 3-D DNA-rods [7], which target application in the far future.

Carbon nanotubes (CNTs) are the most promising nanoelectronic interconnects due to their extraordinary properties such as electrical current carrying capability, mechanical strength, and thermal conductivity. Carbon nanotubes also provide three kinds of carbon nanotube field effect transistors (CNFETs): (1) Shottky barrier based carbon nanotube transistors (SB-CNFETs) including a metal-nanotube-metal junction, which is the most mature CNFET technique but is limited by (a) high metal-nanotube contact resistance and (b) ambipolar behavior, (2) MOSFET-like CNFETs including doped $p(n)$ source and drain regions, which provide high on current, and (3) band-to-band tunneling based carbon nanotube transistors (T-CNFETs) including highly doped $p^+(n^+)$ source and drain regions, which provide ultra low off current suitable for low power applications [20]. CNTs and CNFETs are among the most promising candidates as the building blocks of next generation non-silicon based nanoelec-

Fig. 1. Layers of orthogonal carbon nanotubes form a dense array of RDG-CNFETs and programmable interconnects and constitute a nanoelectronic architecture [10].
tronics systems.

Recently, a CNT crossbar based nano-architecture is proposed which is based entirely on CNTs and CNFETs (Fig. 1) [10]. This nano-architecture achieves expected yield based on the regularity of the crossbar structure, achieves functionality and reliability of nanoelectronic circuits (Fig. 3) by novel reconfigurable double gate carbon nanotube field effect transistors (RDG-CNFTFs) (Fig. 2). It also includes novel voltage controlled nano-addressing circuits (Fig. 4), which achieves expected yield improvement based on the regular layout, and is capable to adapt to parametric variations by the external voltages [11].

Prevalent defects and significant parametric variations are expected in the nanometer domain where the uncertainty principle of quantum physics dominates. As a result, nanoelectronic design must be tolerant to the presence of prevalent defects and significant parametric variations. Complementary to redundant, adaptive, and resilient nanoelectronic design techniques, this requires a predictive nanoelectronic design methodology, e.g., based on a priori defect maps. Existing nano-architecture defect mapping techniques are as follow. (1) On a Teramac reconfigurable computing platform, signals are propagated along each row or each column in a crossbar structure, a defect is located at the intersection of a defective row and a defective column. Here the presence of a single defect is assumed [3]. (2) In the NanoFabric nano-architecture, the (roughly estimated) number of defects for a subset of computing resources are collected by (counter or none-some-many) circuits, a simple graph based algorithm or a Bayes’ rule based probabilistic computation procedure gives defect occurrence probability estimates. (3) More complex BIST methods are also proposed [2].

This paper focuses on CNT crossbar nano-architecture, and proposes a complete set of linear complexity catastrophic defect mapping techniques. This paper also proposes an adaptive CNT matching method for double gate CNFETs in the presence of CNT misalignment. Combined with adaptive nano-addressing method, these proposed techniques enable adaptive configuration of nanoelectronic circuits of correct functionality, performance, and reliability based on the CNT crossbar nano-architecture.

The rest of this paper is organized as follows. Section II briefly reviews the CNT crossbar nano-architecture. Section III presents categorized catastrophic defects in CNT crossbar nano-architecture, and corresponding defect detection and location techniques. Section IV presents process variation effects, and proposes an adaptive CNT matching method which enables nanoelectronic reconfiguration in the presence of RDG-CNFTET front and back gate CNT misalignment. Section V concludes this paper.

II. CNT CROSSBAR NANO-ARCHITECTURE

CNT crossbar nano-architecture is the first nano-architecture which is based entirely on CNTs and CN-
FETs [10]. CNT crossbar nano-architecture consists of layers of orthogonal CNT arrays, where each junction of three layers of doped semiconductive CNTs form a reconfigurable double gate carbon nanotube field effect transistor (RDG-CNFET) (Fig. 2). The top and the bottom carbon nanotubes form the front gate and the back gate, while the doped carbon nanotube in the middle forms the source and the drain of a MOSFET-like CNFET [20]. Electrically bistable (e.g., V-shaped amphiphilic [2]-rotaxane $5^{4+}$ [19]) molecules are sandwiched between the front gate and the source/drain regions, which are electrically reconfigurable to be conductive (and form a via) or insular. Dielectric and redox active (e.g., cobalt phthalocyanine (CoPc) [8]) molecules are sandwiched between the back gate and the source/drain regions, which are electrically reconfigurable to hold/release charge in a redox (reduction/oxidation) process in the back (floating) gate to change the CNFET threshold voltage and conductance.

As a result, a RDG-CNFET is reconfigurable to:

1) Via, by configuring the via forming molecules to be conductive.
2) Short, by configuring the via forming molecules to be insular, and the gate forming molecules to hold positive(negative) charge in a n-type(p-type) CNFET.
3) MOSFET-like CNFET, by configuring the via forming molecules to be insular, and the gate forming molecules to hold negative(positive) charge in a n-type(p-type) MOSFET-like CNFET.
4) Open, by turning off the configured MOSFET-like CNFET by setting the front gate voltage.

At the architecture level, gate forming (dielectric and redox active) molecules and via forming (electrically bistable) molecules need to be evenly distributed between adjacent CNT layers for optimized circuit performance. Via forming (electrically bistable) molecules must be present between any two adjacent layers to provide connectivity between adjacent layers. Gate forming (redox active) molecules must be present next to each layer to provide gate isolation and form opens in interconnects. A top-down (e.g., lithography) process defines the areas for each type of molecules to assemble on each layer. Similar processes define the p- and n-wells for the RDG-CNFETs. Configuration leads to a VLSI circuit including MOSFET-like CNFETs and interconnects with opens, shorts and vias (Fig. 3).

Such carbon nanotube arrays are addressed via the nano interfaces on the boundaries of the crossbar structure, which enables configuration of the architecture (Fig. 1).

Previous binary decoder based nano-addressing circuits [5], [16] require precise layout control to achieve unique physical structure for each nanoscale wire, which seriously limits yield and hinders nano-addressing circuit scaling with the rest of a nanoelectronic system. Alternatively, voltage controlled nano-addressing circuit (Fig. 4) differentiates nanoscale wires by their electrical parameter, in particular, the gate voltage of the pass transistors in the nanoscale wires. By applying an decreasing (increasing) series of pass transistor gate voltages through the voltage divider in the first(second) address line, the pass transistors on the right (left) side in the first(second) address line are turned off, resulting only specific current-carrying nanotube(s) (Fig. 5). Voltage controlled nano-addressing circuits are expected to achieve significant yield improvement, enable aggressive nano-addressing circuit scaling with the rest of a nanoelectronic system, while adaptive application of external voltages is able to precisely address a CNT even in the presence of parametric variations [11].

III. Catastrophic Defects and Mapping Techniques

In this section, we examine catastrophic defects for CNTs, programmable vias and CNFETs, and their corresponding detection and location methods.

A. Metallic, Open and Crossover CNTs

CNTs are metallic or semiconductive depending on their chirality. One third of CNTs are metallic if they are grown isotropically. Metallic CNTs can be removed by either chemical etching [23] or electrical breakdown [1]. However, such techniques bring large process variation effects [13]. Mitra et al. propose use of CNT bundles for each nanoelectronic signal to reduce metallic CNT effect [13]. We observe that metallic CNTs need not necessarily to be removed and CNT bundles are not needed for each nanoelectronic signal as long as metallic CNTs can be detected and located. Upon detection and location, metallic CNTs can be configured to form global interconnects if not avoided. Their low resistivity helps to reduce signal propagation delay in global interconnects which are critical to nanoelectronic circuit performance.

Open CNTs are expected to be prevalent in a CNT array, as open CNT occurrence is proportional to the length of the CNT. A CNT with a single open can be largely included in a correct nanoelectronic design, upon detection and location of the single defect. A CNT with two (or more) opens is not fully utilisable. The segment between the two (extreme) opens are not accessible by any nano-addressing circuit, and components attached to that segment are not configurable. Upon detection and location of the extreme opens, the end segments of an open CNT can be included in a nano-circuit. Or, we can simply avoid open CNTs.

CNTs which are supposedly-parallel may cross over each other, resulting in different addresses for a CNT on two sides of a crossbar, and unexpected resistive
contacts between CNTs. If not corrected by etching [13], such crossover CNTs can be taken as multi-thread cables and included in a correct nano-circuit. It is necessary to solve the following problem for nano electronic circuit configuration on a CNT crossbar nano-architecture.

Problem 1: Detect and locate metallic, open and crossover CNTs in an CNT array, which are addressed on both ends by nano-addressing circuits.

Such metallic, open, and crossover CNTs can be captured in a $n \times n$ resistance matrix $R_{CNT}$, where each entry $R_{CNT}(i,j)$ gives the resistance of CNT between the $i$-th CNT end and the $j$-th CNT end on the opposite sides of an array of $n$ CNTs (if $i \neq j$, $R_{CNT}(i,j)$ gives the resistance of a crossover CNT, otherwise, $R_{CNT}(i,i)$ gives the $i$-th CNT’s resistance).

Method 1 solves Problem 1 by giving such a $n \times n$ resistance matrix $R_{CNT}$. With this CNT resistance matrix $R_{CNT}$, we avoid open CNTs, and consider only semiconductive CNTs, metallic CNTs, and crossover CNT bundles (as multi-thread cables) for the rest of the calibration (Methods 2 and 3 and 4).

### Method 1: Metallic, Open, Crossover CNT Detection and Location

**Input:** Array of $n$ CNTs with nano-addressing circuits on both ends (Fig. 1)

**Output:** Resistance map $R_{CNT}$ for metallic, open, crossover CNTs

1. Configure all CNFETs as shorts
2. For each $i$
3. For each $j$
4. Address the $i$-th CNT on one end of CNT
5. Address the $j$-th CNT on the other end of CNT
6. Measure resistance $R_{CNT}(i,j)$
7. If $i = j$ and $R_{CNT}(i,j) \approx \infty$
8. Open CNT $(i,j)$
9. If $i \neq j$ and $R_{CNT}(i,j) \ll \infty$
10. Crossover CNT $(i,j)$
11. If $R_{CNT}(i,j) \approx R_{metallic}$
12. Metallic CNT $(i,j)$
13. If $R_{CNT}(i,j) \approx R_{semiconductive}$
14. Semiconductive CNT $(i,j)$

### Method 2: Permanently Open or Short Via Detection and Location

**Input:** Two layers of $m \times n$ CNT crossbar with nano-addressing interface on four sides

**Output:** Resistance maps $R_{Pmin}$ and $R_{Pmax}$ for permanently open or short vias

1. For each non-open CNT $i$
2. For each non-open CNT $j$
3. Address $i$-th CNT from top(down) of crossbar
4. Address $j$-th CNT from left(right) of crossbar
5. Program via $V(i,j)$ to conductive
6. Measure path resistance $R_{Pmin}(i,j)$
7. Program via $V(i,j)$ to insular
8. Measure path resistance $R_{Pmax}(i,j)$
9. If $R_{Pmin}(i,j) = R_{Pmax}(i,j) \approx \infty$
10. Permanently open via $V(i,j)$
11. If $R_{Pmin}(i,j) = R_{Pmax}(i,j) \approx R_{CNT}(i,j)$ or $R_{CNT}(j,i)$
12. Permanently short via $V(i,j)$

### C. Opens and Shorts in CNFETs

A CNT junction with dielectric and redox active molecules is supposedly reconfigured as a FET. A catastrophic defect could lead to (1) short between source and drain (e.g., due to channel punchthrough, no intrinsic channel area, redox active molecules cannot release charge), (2) short between gate and source or drain (e.g., due to dielectric breakthrough), or (3) constant open gate (e.g., redox active molecules cannot hold charge). It is necessary to solve the following problem for nano electronic circuit configuration on a CNT crossbar nano-architecture.

Problem 3: Detect and locate permanently open or short CNFETs in a CNT crossbar nano-architecture.

Shorts between CNFET gate and source or drain can be detected in a method which is similar to Method 2 but without via programming. Method 3 finds permanent opens or shorts between the source and the drain of a CNFET by giving a $m \times n$ resistance matrix $R_{CNFET}$. Upon detection and location, these catastrophic defects (metallic, open and crossover CNTs, permanently open or short vias and CNFETs) can be included in a correct nano-circuit. Nano-circuit physical design needs to be adaptive to the presence of these catastrophic defects, and will be different from die to die, based on the catastrophic defect maps ($R_{CNT}$, $R_{Pmin}$, $R_{Pmax}$, and $R_{CNFET}$) for each die.
A. RDG-CNFET Gate CNT Misalignment and Adaptivity in the presence of such process variations. The neighboring CNTs have cross-coupling effect which needs to be simulated/tested or avoided by shielding.

Other process variation effects include CNT resistance and parametric variations in nano-addressing circuits. An adaptive nano-addressing method is able to precisely address a CNT in the presence of such process variations [11]. Other process variations include CNT resistance and capacitance and CNFET driving strength variations. Adaptive or resilient nanoelectronic circuit design techniques are expected to achieve functionality and reliability in the presence of such process variations.

A. RDG-CNFET Gate CNT Misalignment and Adaptive Matching

Another process variation effect is front and back gate CNT alignment in a RDG-CNFET. The CNT forming the front gate and the CNT forming the back gate of a RDG-CNFET may not have the same projection on the middle CNT. This is because that the CNT arrays on different layers do not have and are not expected to have a precise alignment mechanism.

However, an observation is that precise alignment between front gate CNTs and back gate CNTs are not necessarily required as long as the CNT arrays are dense, e.g., with CNT spacing close to CNT diameter. In such a case, a double gate field effect transistor is formed anyway even in the presence of front and back gate CNT misalignment (Fig. 6). The CNFET channels are formed by doping the source/drain regions with the upper layer CNTs as masks. As a result, the CNFET channels align with the front gate CNTs. A misaligned back gate injects a weaker electrical field in the CNFET channel from a longer distance. A neighboring back gate may also injects a weak electrical field in the channel. This is either tolerated (which needs to be verified by simulation or testing) or avoided (by reserving the neighboring back gates for shielding).

The question is then how to find the closest (and the next closest) CNT pair on different layers which form the front gate and the back gate of a RDG-CNFET (such that we can address them and configure the RDG-CNFET).

Problem 4 (Adaptive CNT Matching): Given a CNT i on layer l, locate the closest (and the next closest) CNT j(j') on layer l + 2 (or l – 2) such that CNTs i and j(j') form the front gate and the back gate of a RDG-CNFET.

Method 4 solves Problem 4 and finds the closest CNT pairs.

IV. PARAMETRIC VARIATION AND ADAPTIVE DESIGN

Other than catastrophic defects, process variations are also critical to nanoelectronic circuit performance and reliability. Compared with catastrophic defects, process variations are more prevalent, and they are more difficult to detect since their effects are accumulated in affecting the underlying circuit. Process variations include CNT misalignment and parametric variations in nano-addressing circuits. An adaptive nano-addressing method is able to precisely address a CNT in the presence of such process variations [11]. Other process variations include CNT resistance and capacitance and CNFET driving strength variations. Adaptive or resilient nanoelectronic circuit design techniques are expected to achieve functionality and reliability in the presence of such process variations.

Method 3: Permanently Open or Short CNFET Detection and Location

| Input: | CNFETs in crossbar with nano-addressing interface, CNT resistance matrix $R_{CNT}$ |
| Output: | Resistance map $R_{CNFET}$ for permanently open or short CNFETs |

1) Configure all CNFETs as shorts
2) For each non-open CNT $i$
   4) Address the i-th CNT on both ends
   5) Configure CNFET $(i,j)$ as open
   6) Measure resistance $R_{CNFET}(i,j)$
   7) If $R_{CNFET}(i,j) \approx R_{CNT}(i,j) < \infty$
   8) Short between CNFET $(i,j)$ source-drain
   9) If $R_{CNFET}(i,j) \approx R_{CNT}(i,j) \approx \infty$
   10) Open between CNFET $(i,j)$ source-drain
11) Configure CNFET $(i,j)$ as short

Once a matching back gate is identified, the CNFET can be characterized (by achieving its I-V curves). The parasitic effect of a neighboring back gate can also be characterized (by achieving its I-V curves), which is then either tolerated or avoided in a nanoelectronic design.

B. Function and Performance Calibration and Adaptive Configuration

In adaptive configuration, each module of the circuit is configured with its test circuit. The test circuit can
be as simple as additional interconnects which connect the inputs and the outputs of the module to some of the primary inputs and the primary outputs, respectively. In such cases, function and performance calibration is performed externally. Alternatively, self-test can be performed given the complexity of the test circuit. If the current configuration passes online function and performance verification, the auxiliary test circuit will be removed, and the current configuration of the module is committed. Otherwise, the same circuit module needs to be realized using other hardware resources on the reconfigurable platform.

V. Evaluation and Conclusion

This paper proposes a set of catastrophic defect mapping techniques, which are specific (to the CNT crossbar nano-architecture), complete (in detecting and locating all possible catastrophic defects in the CNT crossbar nano-architecture), deterministic (with no probabilistic computation), and efficient (test paths are rows or columns of CNT, or L-shaped CNT paths, CNT open/short defect detection is separated with via/CNFET open/short defect detection, runtime is linear to the number of defect sites). This is significant improvement compared with previous techniques (e.g., the Teramac technique [3] detects only a single defect, the NanoFabric technique [12] is generic, abstract, probabilistic, and highly complex).

This paper also proposes an adaptive CNT matching method, which enables nanoelectronic circuit configuration even in the presence of CNT misalignment. This adaptive CNT matching technique and the adaptive addressing technique for the voltage-controlled nano-addressing circuit [11] form a complete set of addressing and configuration techniques which are adaptive to process variations in a CNT crossbar nano-architecture.

These proposed techniques are expected to enable adaptive configuration of nanoelectronic circuits of correct functionality, performance, and reliability based on the CNT crossbar nano-architecture. Compared with previous techniques (e.g., [13]), the proposed techniques achieve improved applicability (e.g., without the need of etching for layout correction) and scalability (e.g., without the need of CNT bundles for every signal).

Ongoing research explores function and performance calibration of nanoelectronic circuit modules.

References