

EE3563 Digital Systems Design (Fall 2009 MW 7:00-8:15pm **EB 2.04.22**)

Instructor: Dr. Byeong Kil Lee
Office: BSE 4.312 (temporary)
Office hours: M: 1-3pm, W: 10am-12pm or by appointment
E-mail: byeong.lee@utsa.edu
URL: <http://engineering.utsa.edu/~blee>
Course Description: Introduction to switching theory; design of complex combinational and sequential circuits; analysis of hazards and fault detection, location, and tolerance; design and verification of complex circuitry using schematic entry; functional modeling, and mixed-mode simulation
Prerequisites: EE 2511 and EE 2513 (Logic design / Lab)

Textbook: Digital System Design Using VHDL, 2nd edition
(C. H. Roth and L. K. John)

Reference books:
Digital System Design with VHDL, 2nd edition by Mark Zwolinski
VHDL : Programming By Example by Douglas Perry

TA/grader: Satish Raghunath

Lab: The course has a lab component (VHDL and FPGAs). The primary lab is **EB 2.04.22**. Lab includes VHDL simulation, VHDL Synthesis and Designing on FPGAs, etc.
Lab hours: Thu/Fri **9am-noon**, TA/grader will be available in the EB 2.04.22 (In some cases, instructor/TA will do lab-related lecture)
Tools:

- Modelsim
- Xilinx Spartan FPGA board / ISE

Homework and Lab Assignments: 5 & 5

GRADING: *(tentative)*

Homework & Lab assignments	25%
Midterm Exams (2)	40% (20% each)
Final Exam	30%
Class Participation, Pop quizzes, etc.	5%

Attendance Policy: Attendance is required. Students are responsible for topics covered in missed classes, as well as any assignments due.

Academic Integrity and Collaboration: Cheating in any form will be fully prosecuted. Collaboration is allowed on homework assignments, but the submission must be each student's own work.

Pop quizzes: There will be quizzes during the semester. No makeups allowed on pop quizzes, but extra credit from labs can compensate for credit lost in quizzes.

In classroom: No disruptive activity/talking amongst students in class during lectures. If you have a question on the material, ask the instructor. Be professional in your behavior in class. Disruptive activity can lead to grade penalties.

The University of Texas at San Antonio provides, upon request, appropriate academic adjustments for qualified students with disabilities. For more information, visit Disability services homepage (<http://www.utsa.edu/disability/>) or call to (210) 458-4157

Schedule (tentative):

Wk	Dates	Topics	Notes
1	08.26	Course overview, Design flow	
2	08.31 09.02	Logic design fundamentals	
3	09.07 09.09	No class (Labor day) Intro to VHDL	
4	09.14 09.16		
5	09.21 09.23	Programmable logic Design examples	
6	09.28 09.30	/ Review	
7	10.05 10.07	Midterm-I (tentative) Digital design with state machine charts	
8	10.12 10.14	Design with FPGA	
9	10.19 10.21	Floating-point arithmetic	
10	10.26 10.28	/ Review	
11	11.02 11.04	Midterm-II (tentative) Additional topics in VHDL	
12	11.09 11.11		
13	11.16 11.18	RISC microprocessor	
14	11.23 11.25	Hardware testing and DFT	
15	11.30 12.02	Additional design examples Verilog tutorials (if time allows)	
16	12.07 12.09	No class (student study day) Final exam	

Links:

Fall 2009 Calendar: http://www.utsa.edu/registrar/reg_materials/reg_calendar_fall.pdf

WebCT: <https://webct.utsa.edu>