

CURRICULUM VITAE

Name: Bao Liu
Rank: Assistant Professor

I. GENERAL INFORMATION

A. Personal Data:

- Born Oct. 1973.

B. Education:

- Ph.D., Computer Science, UC San Diego, 2003
- M.S., Electrical Engineering, Fudan University, China, 1996
- B.S., Electrical Engineering, Fudan University, China, 1993

C. Academic Appointments (chronological with latest first):

- UT San Antonio Assistant Professor 2008-
- UC San Diego, Post-Doctoral Researcher, 2005-2008

D. Other Employment:

- Cadence Design Systems, Senior Technical Staff, 2004-2005
- Incentia Design Systems, Senior Engineer, 2002-2004
- Conexant Systems, Inc., Intern, 2000
- Cadence Design Systems, Intern, 1999
- China IC Design Center, Senior Engineer, 1996-1998

E. Consulting:

- Blaze DFM, Consultant, 2005

F. Certification and Licensure:

G. Honors and Awards

- Best Paper, International Conference on Computer Design, 2005
- Best Poster, UCSD Research Review, 2001
- Best User, China ICCAD Association, 1996
- Honor Medal, China Mathematics Olympiad, 1988

II. TEACHING

1) Classroom/Laboratory:

<u>Date</u>	<u>Course</u>	<u>Level</u>
Fall 2008	UTSA EE5323 Advanced VLSI Design	<u>G</u>
Winter 2006	UCSD CSE241A/ECE260B VLSI Design Methodology	<u>G</u>

Level: Undergraduate (U), Graduate (G)

B. Instructional Development:

1. Courses Developed (Course number, title, date)

UTSA EE5323	Advanced VLSI Design	Fall 2008
UCSD CSE241A/ECE260B	VLSI Design Methodology	Winter 2006

2. Media and Software Developed

C. Masters' Theses and Ph.D. Dissertations Directed

1. Masters

2. Ph.D. Dissertation

D. Membership on Graduate Committees

1. Masters

2. Ph.D. Dissertation

E. Postdoctoral Fellows Supervised

F. Undergraduate Students (Research) Supervised

III. RESEARCH

A. Bibliography:

1. Books/Book Chapters

1a. Books

1b. Book Chapters

2. Journal Papers (refereed full length)

2a. Published or In Press

- 1) B. Liu and S. X.-D. Tan, "Efficient Decoupling Capacitor Insertion in VLSI Power/Ground Networks by Semidefinite and Linear Programs," *IEEE Trans. on VLSI Systems*, 15(11), 2007, pp. 1284-1287.
- 2) A. B. Kahng, B. Liu, and Q. Wang, "Stochastic Power/Ground Supply Voltage Prediction and Optimization via Analytical Placement," *IEEE Trans. on VLSI Systems*, 15(8), 2007, pp. 904-912.
- 3) A. B. Kahng, B. Liu, and X. Xu, "Statistical Timing Analysis in the Presence of Signal Integrity Effects," *IEEE Trans. on Computer-Aided Design*, 26(10), 2007, pp. 1873-1877.
- 4) A. B. Kahng, B. Liu and I. Mandoiu, "Non-tree Routing for Reliability and Yield Improvement," *IEEE Trans. on Computer-Aided Design*, 23(1), 2004, pp.148-156.
- 5) C. Albrecht, A. B. Kahng, B. Liu, I. Mandoiu and A. Zelikovsky, "On the Skew-Bounded Minimum-Buffer Routing Tree Problem," *IEEE Trans. on Computer-Aided Design*, 22(7), 2003, pp. 937-945.
- 6) C. Alpert, A. B. Kahng, B. Liu, I. Mandoiu and A. Zelikovsky, "Minimum Buffered Routing with Bounded Capacitive Load for Slew Rate and Reliability Control," *IEEE Trans. on Computer-Aided Design*, 22(3), 2003, pp. 241-253.
- 7) C. J. Alpert, G. Gandham, M. Hrkic, J. Hu, A. B. Kahng, J. Lillis, B. Liu, S. T. Quay, S. S. Sapatnekar and A. J. Sullivan, "Buffered Steiner Trees for Difficult Instances," *IEEE Trans. on Computer-Aided Design*, 21(1), 2002, pp. 3-14.
- 8) C.-K. Cheng, A. B. Kahng, B. Liu and D. Stroobandt, "Toward Better Wireload Models in the Presence of Obstacles," *IEEE Trans. on VLSI Systems*, 10(2), 2002, pp. 177-188.

2b. Submitted/Under Preparation.

- 1) B. Liu, "Robust Asynchronous Nanoelectronic Circuits," *IEEE Trans. on VLSI (to submit)*, 2009.
- 2) B. Liu, "Reconfigurable Double Gate Carbon Nanotube Based Nanoelectronic Architecture," *IEEE Trans. on Emerging Technologies (to submit)*, 2009.

- 3) B. Liu, "Signal Probability Based Statistical Timing Analysis," *IEEE Trans. on CAD (to submit)*, 2009.
- 4) B. Liu and S. X.-D. Tan, "Scalable Frequency Analysis of Nanometer VLSI System Power Delivery Network via Stochastic Moment Matching," *Integration, VLSI Journal (submitted)*, 2009.

3. Conference Papers

3a. Published or Accepted

- 1) B. Liu, "Reconfigurable Double Gate Carbon Nanotube Transistor Based Nanoelectronic Architecture," *Proc. Asia and South Pacific Design Automation Conference (to appear)*, 2009.
- 2) B. Liu, "Voltage Controlled Carbon Nanotube Addressing Circuit," *Proc. International Conference on Nano-Networks*, 2008.
- 3) B. Liu, "Performance Variation Adaptive Differential Signaling via Carbon-Nanotube Bundles," *Proc. International Conference on Solid-State and Integrated-Circuit Technology*, 2008.
- 4) B. Liu, "Analog/RF Design Techniques for High Performance Nanoelectronic On-Chip Interconnects," *Proc. International Conference on Solid-State and Integrated-Circuit Technology*, 2008.
- 5) B. Liu, "Signal Probability Based Statistical Timing Analysis," *Proc. Design Automation & Test in Europe*, 2008, pp. 562-567.
- 6) B. Liu, "Spatial Correlation Extraction via Product Chip Performance Statistics," *Proc. Design Automation & Test in Europe*, 2008, pp. 527-532.
- 7) A. B. Kahng, S. M. Kang, W. Li and B. Liu, "Efficient Analytical Placement for VLSI Lifetime and Reliability Improvement and Minimum Performance Variation," *Proc. International Conference on Computer Design*, 2007, pp.71-77.
- 8) X. Yuan, J. Fan, B. Liu and S. X.-D. Tan, "Stochastic Based Extended Krylov Subspace Method for Power/Ground Network Analysis," *Proc. International Conference on ASIC*, 2007.
- 9) B. Liu, "Statistical Gate Level Simulation Based on Parameterized Models for Process and Signal Variations," *Proc. International Symposium on Quality Electronic Design*, 2007, pp. 257-261.
- 10) B. Liu, A. B. Kahng, X. Xu, J. Hu and G. Venkataraman, "A Global Minimum Clock Distribution Network Augmentation Algorithm for Guaranteed Clock Skew Yield," *Proc. Asia and South Pacific Design Automation Conference*, 2007, pp. 24-31.
- 11) B. Liu and A. B. Kahng, "Statistical Gate Level Simulation via Voltage Controlled Current Source Models," *Proc. Behavior Modeling and Simulation Workshop*, 2006, pp. 23-27.
- 12) B. Liu and A. B. Kahng, "Expected Performance Centering for Analog/RF Design," *Proc. Behavior Modeling and Simulation Workshop*, 2006, pp. 126-131.
- 13) B. Liu, "Stochastic Power/Ground Supply Voltage Analysis via Moment and Correlation Computation by Statistical Transient Toggling Analysis," *Proc. Electronic Design Processes Workshop*, 2006.
- 14) A. B. Kahng, B. Liu and X. Xu, "Statistical Gate Delay Calculation with Crosstalk Alignment Consideration," *Proc. Great Lakes Symposium on VLSI*, 2006, pp. 223-228.
- 15) A. B. Kahng, B. Liu and X. Xu, "Statistical Crosstalk Aggressor Alignment Aware Interconnect Delay Calculation," *Proc. System-Level Interconnect Prediction*, 2006, pp. 91-97.
- 16) A. B. Kahng, B. Liu and S. Tan, "Efficient Decoupling Capacitor Planning via Convex Programming Methods," *Proc. ACM/IEEE International Symposium on Physical Design*, 2006, pp. 102-107.
- 17) A. B. Kahng, B. Liu and S. Tan, "SMM: Scalable Analysis of Power Delivery Networks by Stochastic Moment Computation," *Proc. International Symposium on Quality Electronic Design*, 2006, pp. 638-643.
- 18) A. B. Kahng, B. Liu and X. Xu, "Constructing Current-Based Gate Models based on Existing Timing Libraries," *Proc. International Symposium on Quality Electronic Design*, 2006, pp. 37-42.
- 19) A. B. Kahng, B. Liu and Q. Wang, "Supply Degradation Aware Placement," *Proc. International Conference on Computer-Aided Design*, 2005, pp. 437-443. (**Best Paper Award**, 5 out of 337 submission)
- 20) A. B. Kahng and B. Liu, "Q-Tree: A New Iterative Improvement Approach for Buffered Interconnect Optimization," *Proc. Computer Society Annual Symposium on VLSI*, 2003, pp. 183-188.
- 21) A. B. Kahng, B. Liu, and I. Mandoiu, "Non-Tree Routing for Reliability and Yield Improvement," *Proc. International Conference on Computer-Aided Design*, 2002, pp. 260-266.
- 22) C. Albrecht, A. B. Kahng, B. Liu, I. Mandoiu and A. Zelikovsky, "On the Skew-Bounded Minimum Buffer Routing Tree Problem," *The Tenth Workshop on Synthesis and System Integration of Mixed Technologies*, 2001, pp. 250-256.

- 23) C. J. Alpert, A. B. Kahng, B. Liu, I. Mandoiu, J.-D. Nale and A. Zelikovsky, "Minimum-Buffered Routing of Non-Critical Nets for Slew Rate and Reliability Control," *Proc. Intl. Conference on Computer-Aided Design*, 2001, pp. 408-415.
- 24) C. J. Alpert, G. Gandham, J. Hu, S. T. Quay, A. J. Sullivan, M. Hrkic, J. Lillis, A. B. Kahng, B. Liu and S. Sapatnekar, "Buffered Steiner Trees for Difficult Instances," *Proc. International Symposium on Physical Design*, 2001, pp. 4-9.
- 25) C.-K. Cheng, A. B. Kahng and B. Liu, "Interconnect Implications of Growth-Based Structural Models for VLSI Circuits," *Proc. International Workshop on System-Level Interconnect Prediction*, 2001, pp. 99-106.
- 26) C.-K. Cheng, A. B. Kahng, B. Liu and D. Stroobandt, "Toward Better Wireload Models in the Presence of Obstacles," *Proc. Asia and South Pacific Design Automation Conference*, 2001, pp. 527-532.

3b. Submitted/Under Preparation

- 1) B. Liu, "Robust Differential Asynchronous Nanoelectronic Circuits," *Proc. International Symposium on Quality Electronic Design (submitted)*, 2009.
- 2) B. Liu, "Adaptive Implementation for Robust Molecular Circuits Based on a Self-Calibrated Reconfigurable Computing Platform," *Proc. Design Automation and Test in Europe (submitted)*, 2009.

4. Book Reviews

5. Other Articles

- 1) B. Liu, X. Xu, and A. B. Kahng, "SSTA-SI: Signal Integrity Effects Aware Statistical Static Timing Analysis," *UCSD Technical Report CS2007-0883*.
- 2) B. Liu, "Maximum Instantaneous Power Estimation by Subgraph Coloring," *UCSD Technical Report CS2005-0834*.
- 3) B. Liu, "Charge Matching Based Tail Approximation in a Piecewise Linear-and-Exponential Function," *UCSD Technical Report CS2005-0835*.
- 4) B. Liu, "NP-Completeness and Approximation Scheme of Zero-Skew Clock Tree Problem," *UCSD Technical Report CS2005-0837*.

B. Lectures, Seminars

(Chronologically, NOT INCLUDING presentations given at conferences as shown in 3a)

1. Scientific Lectures, Seminars

- 1) B. Liu, "Novel Design for Manufacturing Techniques," Tsinghua University, Beijing, Oct. 2008.
- 2) B. Liu, "Towards Robust, High Performance and Low Power Nanoelectronic Circuits," Fudan University, Shanghai, Oct. 2008.
- 3) B. Liu, "Statistical VLSI Design Analysis", University of California Riverside Electrical Engineering Department Colloquium, 2006.
- 4) B. Liu, "Non-Tree Routing for Reliability and Yield Improvement", University of California San Diego Computer Science and Engineering Department Seminar, 2006.
- 5) B. Liu, "Signal Integrity Aware Physical Design", Qualcomm Corporation visit, 2005.

2. Other Lectures, Seminars, Briefings, Short courses

C. Areas of Research Interest

- Nanoelectronic Architecture
- Robust Nanoelectronic Design
- Nanoelectronic Variability and Reliability Analysis
- Biomedical Engineering

D. Research Support

1. National/International

Agency:
Title:
Peer Reviewed (Y/N)
Date (start-end)
Total amount:
Role (Principal Investigator/Co-Investigator)

(Repeat for each grant)

2. State

Agency:
Title:
Peer Reviewed (Y/N)
Date (start-end)
Total amount:
Role (Principal Investigator/Co-Investigator)

(Repeat for each grant)

3. Companies

Agency:
Title:
Peer Reviewed (Y/N)
Date (start-end)
Total amount:
Role (Principal Investigator/Co-Investigator)

(Repeat for each grant)

4. Other including sub-contracts, internal UTSA funding through earmarks, institutional grants etc.

Agency:
Title:
Peer Reviewed (Y/N)
Date (start-end)
Total amount:
Role (Principal Investigator/Co-Investigator)

(Repeat for each grant)

5. Pending with funding agency

Agency:
Title:
Peer Reviewed (Y/N)
Date (start-end)
Total amount:
Role (Principal Investigator/Co-Investigator)

(Repeat for each grant)

IV. SERVICE

A. Professional Activities:

1. Current Professional and Scientific Organizations/Societies If election/nomination required then mark with *

Years (from-to)	Name of Organization
2000 – present	IEEE

2. Past and Current Positions and/or Offices Held in Professional Organizations

Years (from-to)	Name of Organization	Position held
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3. Other Professional Activities (e.g., National and State Consultantships, Review Panels and Committees, Editorial Boards, Continuing Education Lectures Presented, etc.)

Editor/Editorial Board Member

Meeting/Symposium Organizer/Chairmanship

Meeting

Year

Role

Session Chair/Organizer

Year, Meeting, Session Name

(Repeat for each session)

Co-Chair, 2006-present, International Symposium on Quality Electronic Design (ISQED), Emerging Design and Technology (EDT) subcommittee

Reviewer for Journals

Name of Journal

IEEE Trans. on Computer-Aided Design, IEEE Trans. on VLSI Systems, IEEE Trans. on Circuits and Systems (TCAS-I, TCAS-II), International Journal of Computers and Electrical Engineering

Review Panels (for grants)

Year, Agency, Panel Name

(Repeat as necessary)

Continuing Education Seminars Given

Date, Seminar name

4. Community Service

Date, Service, Agency

B. Committees:

1. Department (specify if Chair)

Year, Committee

(Repeat as necessary)
ABET PEO Assessment Committee

2. College of Engineering (*specify if Chair*)
Year, Committee
(Repeat as necessary)

3. University (*specify if Chair*)
Year, Committee
(Repeat as necessary)

4. Other
Year, Committee
(Repeat as necessary)

C. Administrative Responsibilities:

1. Department
Year, Title
(Repeat as necessary)

2. College
Year, Title
(Repeat as necessary)

3. University
Year, Title
(Repeat as necessary)

4. Staff Currently Supervised (not including students):

V. OTHER INFORMATION

A. Patents Pending/Issued:

B. Media Coverage

C. Other