

Curriculum Vitae

Eugene John

Professor

Department of Electrical and Computer Engineering
The University of Texas at San Antonio
San Antonio, TX 78249

I. General Information:

A. Personal Data:

Eugene John
Professor
Department of Electrical and Computer Engineering
Phone: 210 458 5590
Email: Eugene.john@utsa.edu

B. Education:

Ph. D. Electrical Engineering, The Pennsylvania State University, May 1995,
GPA -4.0/4.0

M.S. Electrical Engineering, The University of Texas at El Paso,
August 1990, GPA - 4.0/4.0

B. Sc (Engg) Electronics and Communications Engineering,
The University of Kerala, India, August 1984. First Class

C. Academic Appointments:

9/07 – Present Professor, Electrical and Computer Engineering,
The University of Texas at San Antonio.

9/01- 8/07 Associate Professor, Electrical and Computer Engineering,
The University of Texas at San Antonio.

9/00 – 08/01 Associate Professor, Electrical Engineering,
The University of Texas - Pan American.

8/95 - 8/00 Assistant Professor, Electrical Engineering,
The University of Texas - Pan American.

D. Other Employment:

Summer 96 Summer position at INTEL Corporation in Chandler, Arizona.
Summer 97 Summer position at INTEL Corporation in Chandler, Arizona.

E. Honors and Awards:

One of my graduate students (Dhiresha Kudithipudi) won 1st place in Doctoral Level category in Spring 2006 UTSA College of Engineering Graduate Research Day competitions.

One of my graduate students (Naveena Marupudi) won 2nd place in Masters Level category in Spring 2006 UTSA College of Engineering Graduate Research Day competitions.

One of my graduate students (Ramakrishna Kota) won 1st place in Masters Level category in Spring 2005 UTSA College of Engineering Graduate Research Day competitions.

Presidential Outstanding Faculty Award for Research, The University of Texas - Pan American, 1999.

Elevated to Senior Member Status in IEEE in December 1997.

Scholar's Fund Award, The University of Texas - Pan American, Fall 1998.

Cotton Scholarship awarded by the Graduate School, The University of Texas at El Paso, 1989.

Schellenger Research Scholarship Awarded by the Electrical Engineering Department, The University of Texas at El Paso, Summer 1989.

Who's Who in American Colleges and Universities, 1989-1990.

Member Eta Kappa Nu

Member Tau Beta Pi

Member Phi Kappa Phi.

II. Teaching:

A. Classroom/Laboratory

Spring 2007

EE 4513 Introduction to VLSI Design
EE 5223 Low Power VLSI Design

Fall 2007

EE 4513 Introduction to VLSI Design
EE 5113 VLSI System Design

B. Instructional Development:

Courses Developed

EE 5223 Low Power VLSI Design
EE 5323 Superscalar Processor Design

C. Masters' Theses and Ph.D. Dissertations Directed

1. Masters Theses:

Nagaraju, Tilak Kumar D., Fall 2008
Thesis Title: Design and Implementation of Low Power Phase Locked Loops Circuits for Wireless Applications

Rajesh Vallepalli, Graduated in Summer 2007
Thesis Title: *Low Power RF Front-End using Reflex Concept*

Naveena Marupudi: Fall 2006
Thesis Title: *Finger Print Verification Based on Image Filtering of Ridges*

Pradeep Nair, Graduated in Summer 2005
Thesis Title: *Workload Characterization of Sequence Aligning Bioinformatics Applications*

Juan Portillo, Graduated in Summer 2005
Thesis Title: *Implementation of Fatigue Analysis for Lifetime Prediction on TMS320C67XX DSP Processors*

Ramakrishna Kota, Graduated in Fall 2005

Thesis Title: *Characterization of Arithmetic Circuits for Deep Submicron Chip Design*

Stefan Petko, Graduated in Summer 2003

Thesis Title: *Memory System Characterization for Multimedia Applications*

2. Ph. D. Dissertation:

Dhiresha Kudithipudi, Graduated in Summer 2006

Leakage Power Characterization and Optimization in Nanoscale CMOS Design

(Dr. Kudithipudi is currently an Assistant Professor at Rochester Institute of Technology, Rochester, New York)

D. Membership on Graduate Committees

1. Masters
2. Ph.D. Dissertation

E. Undergraduate Students (Research) Supervised

Ryan Sweet
Ernesto Padilla
Raul Montenegro

III. Research:

A. Bibliography

1. Books:

E. John and J. Rubio, “Unique Chips and Systems” edited book; CRC Press, November 2007

Book Chapters:

E. John, “Semiconductor Memory Circuits”, in the *Computer Engineering Hand Book*, 2nd ed. Editor: V. Oklobdzija, CRC Press, manuscript submitted to the publisher, Invited Chapter, to be published in January 2008

E. John, “VLSI Circuits”, in the *Computer Engineering Hand Book*,

Editor: V. Oklobdzija, CRC Press, pp. 2.1 – 2.20, 2002

L. John and **E. John**, “Bit-Slice Computers”, in the *Encyclopedia of Electrical and Electronics Engineering*, Supplement 1, Editor: J.G.Webster, John Wiley and Sons, Inc. pp. 39-44, 1999.

2. Journal Papers:

Published or in Press

D. Kudithipudi, S. Petko and **E. John** “Cache Design for Multimedia Workloads: Power and Energy Tradeoffs”, *IEEE Transactions on Multimedia*, Vol. 10, No. 6, pp. 1013 – 1021 October, 2008.

C. B. Smith, D. R. Mandel and E. John, “A Superscalar Simulation Employing Poisson Distributed Stalls”, *International Journal of Computers and Electrical Engineering*, pp. 192 – 201, Vol. 34, No. 3, May 2008.

C. Martinez, M. Pinnamaneni and **E. John** "Performance of Commercial Multimedia Workloads on the Intel Pentium 4: A Case Study", Accepted for publication in *International Journal of Computers and Electrical Engineering* (accepted on Feb 6, 2008)

P. S. Nair and **E. John**, “Analyzing the Performance of Personal Computers based on Intel microprocessors for Sequence Aligning Bioinformatics Applications” *International Journal of Bioinformatics Research and Applications*, Vol. 3, No.2, pp. 187-205, 2007

D. Kudithipudi and E. John, “Static Power Analysis and Estimation in TCAM cells”, *Journal of Low Power Electronics*, Vol. 3, pp. 293 – 301, 2007

D. Kudithipudi and **E. John**, “Implications of Gated-Vss Technique on Leakage Power in Embedded Caches” Accepted, *International Journal of Embedded Systems*.

B. K. Lee, L. K. John and **E. John**, “Architectural Enhancements for Network Congestion Control Applications” *IEEE Transactions on VLSI Systems*, Vol. 14, No. 6, pp. 609-615, June, 2006

D. Kudithipudi and **E. John** "Implementation of Low Power Digital Multipliers using 10 Transistor Adder Blocks", *Journal of Low Power Electronics*, Vol. 1, pp. 286 – 296, 2005

A. Moreno and **E. John**, "A Flexible Design for Timing Signals Generation for the Conversion of Computer Video Formats to SDTV 480P", *IEEE Transactions on Consumer Electronics* pp.1081-1086, Vol. 45, November 1999.

L. K. John and **E. John**, "A Dynamically Reconfigurable Interconnect for Array Processors", *IEEE Transactions on VLSI Systems*, Vol. 6, No. 1, pp. 150-157, March 1998.

P. T. Hulina, L. D. Coraor, L. Kurian, and **E. John**, "Design and VLSI Implementation of an Address Generation Coprocessor", *IEE Proceedings on Computers and Digital Techniques*, Vol 142, No. 2, pp. 145- 151, March 1995.

M. B. Das, J. W. Chen, and **E. John**, "Design of Optoelectronic Integrated Circuit Receivers for High Sensitivity and Maximally Flat Frequency Response", *IEEE/OSA Journal of Lightwave Technology*, Vol. 13, No.9, pp. 1876-1884, 1995.

E. John and M. B. Das, "Design and Performance Analysis of InP-Based High-Speed and High Sensitivity Optoelectronic Integrated Receivers", *IEEE Transactions on Electron Devices*, Vol. 42, No. 2, pp. 162-172, 1994.

P. T. Hulina, L. Kurian, **E. John** and L. D. Coraor, "Design and VLSI Implementation of an Access Processor for a Decoupled Architecture", *Journal of Microprocessors and Microsystems*, Vol. 16, No. 5, pp. 237-247, May 1992.

E. John and M. B. Das, "A New Design Approach for a High Transimpedance and Low-Noise Optoelectronic Integrated Lightwave Receiver with 24GHz Bandwidth" *Microwave and Optical Technology Letters*, Vol. 7, No.6, pp. 259-262, April 1994.

E. John and M. B. Das, "Speed and Sensitivity Limitations of Optoelectronic Receivers Based on MSM Photodiode and Millimeter Wave HBTs on InP Substrate", *IEEE Photonics Technology Letters*, vol. 4, No. 10, pp 1145-1148, 1992.

Submitted/Under Preparation

P. S. Nair, **E. John** and F. Hudson, "Execution Characteristics of Embedded Applications on Pentium – 4 Architecture", submitted to *International Journal of Embedded Systems*

3. Conference Papers:

Published or Accepted:

D. Kudithipudi, and **E. John**, "On Estimation of Static Power-Performance in TCAM" *51st IEEE Midwest Symposium on Circuits and Systems*, pp.783-786 MWSCAS'08, August 10 – 13, 2008.

A. Hussein, H. Saleh, B. Mohammad, and **E. John**, "Optimum Organization of SRAM-based Memory for Leakage Power Reduction" *51st IEEE Midwest Symposium on Circuits and Systems*, pp.775-778 MWSCAS'08, August 10 – 13, 2008.

P. Nair, S. Eratne, and **E. John**, "Topology-related effects of Gated- V_{dd} and Gated- V_{ss} techniques on full-adder Leakage and Delay at 65nm and 45 nm", in *Proc. IEEE Asia-Pacific Conf. on Circuits and Systems (APCCAS '08)*, 2008, pp. 972-975.

S. Eratne, S. Puthenpurayil, **E. John**, "Energy Efficient Lossless Image Compression," in *2008 IEEE Asia Pacific Conference on Circuits and Systems*, Macao, China, 2008, pp. 344-347

P. Nair, S. K. K. Venkataswamy, S. Eratne and **E. John**, "Impact of High-K Dielectric Transistors on Full-Adder Delay and Leakage Characteristics", in *Proc. IASTED Int. Conf. Circuits and Systems (CS '08)*, 2008, pp. 55-60.

S. Eratne, S. Puthenpurayil, **E. John**, "Energy Efficiency of Data Compression with Wavelets", *2008 International Conference on Image Processing, Computer Vision, and Pattern Recognition WORLDCOMP'08*, Las Vegas, NV, 2008

P. Nair, S. Eratne, **E. John**, "Effects of Register File Organization on Leakage Power Consumption," *2008 International Conference on Computer Design WORLDCOMP'08*, Las Vegas, NV, 2008

S. Eratne, P. Nair and **E. John**, "Leakage current control of nanoscale full adder cells using input vectors", *IEEE International Conference on Design & Technology of Integrated Systems*, pp. 185 – 189, DTIS'07, Rabat, Morocco, September 2007.

D. Kudithipudi, P. Nair and **E. John**, "On Estimation and Optimization of Leakage Power in CMOS Multipliers" *IEEE Midwest Symposium on Circuits and Systems, MWSCAS'07*, August 2007.

P. Nair and **E. John**, "Performance Analysis of an Intel Pentium-4-based Personal Computer for Multiple Sequence Alignment" *International Conference on Computer Design, CDES'07*, Las Vegas, NV, June 2007.

R. Vellapalli, **E. John**, R. Kuzet, and H. Foltz "Low Power RF CMOS Receiver Front-end Using Reflex Amplifier" The International Signal Processing Conference, Santa Clara, California, October 30-November 2, 2006.

N. Marupudi, **E. John** and F. Hudson, "Fingerprint Verification Based on Image Filtering of Ridges" The International Signal Processing Conference, Santa Clara, California, October 30-November 2, 2006.

J. Tang, F. Hudson and **E. John**, "Remote Fingerprint Entry Verification Using Bluetooth Wireless Technology" The International Signal Processing Conference, Santa Clara, California, October 30-November 2, 2006.

P. S. Nair, D. Kudithipudi, **E. John** and F. Hudson, "Performance Analysis of Embedded Applications on a Pentium-4 Based Machine" *ESA'06 - The 2006 International Conference on Embedded Systems & Applications*, Las Vegas, Nevada, June 26-29, 2006

P. S. Nair and **E. John**, "Performance of Sequence Alignment Bioinformatics Applications on General Purpose Processors: A Case Study" *BIOCOMP'06- The 2006 International Conference on Bioinformatics & Computational Biology*, Las Vegas, Nevada, June 26-29, 2006

C. Martinez, M. Pinnamaneni and **E. John**, "Multimedia Workloads versus SPEC CPU2000", *2006 SPEC Benchmark Workshop*, Austin, TX, January 23, 2006

P. Nair, D. Kudithipudi and **E. John**, "Design and Implementation of a CMOS Non-Restoring Divider", *IEEE Region 5 Conference*, San Antonio, TX, April 6- 8, 2006

N. Marupudi, **E. John** and F. Hudson "Fingerprint Verification in Multimodal Biometrics", *IEEE Region 5 Conference*, San Antonio, TX, April 6- 8, 2006.

S. Eratne, D. Kudithipudi and **E. John**, "Performance Analysis of Full Adders in Nanoscale CMOS Design", *IEEE Region 5 Conference*, San Antonio, TX, April 6- 8, 2006.

R. Kuzet, M. Chilikuri, H. Foltz and **E. John**, "RF CMOS Self-Oscillating Gilbert Cell Mixer", Proceedings of IASTED International Conference on Circuits, Signals, and Systems (CSS 2005), October 24 - 26, 2005, in Marina Del Rey, USA

D. Kudithipudi and **E. John**, "Parametrical Characterization of Leakage Power in Embedded System Caches using Gated-Vss", Proceedings of International Association of Science and Technology for Development on Circuits, Signals and Systems, Marina Del Rey, October 2005

D. Kudithipudi and **E. John**, "A Combinatorial Approach to Suppress Leakage in Nanoscale SRAM Cells", in the proceedings of *IEEE Midwest Symposium on Circuits and Systems-2005*, Cincinnati, Ohio, August 2005.

B. K. Lee, L. K. John and **E. John**, "Architectural Support for Accelerating Congestion Control Applications in Network Processors" *IEEE 16th International Conference on Application-specific Systems, Architectures and Processors (ASAP 2005)*. Greece, July 2005.

D. Kudithipudi and **E. John**, "A Framework to Moderate Leakage Power in Nanoscale CMOS SoC Devices", Poster Presentation, *NanoSummit Research Conference*, Houston, July 2005.

D. Kudithipudi and **E. John**, "Parametrical Characterization of leakage power in Nanoscale Technologies", Poster Presentation, *IBM's Austin Conference on Energy Efficient Design*, March 2005.

D. Kudithipudi, S. Petko and **E. John**, “Cache leakage power Analysis in Embedded Application” in proceedings of IEEE Midwest Symposium on Circuits and Systems, Hiroshima, Japan, Vol. II, pp. 517-520, 2004.

D. Kudithipudi, R. Kota, **E. John** and Z. P. Tanner, “Impact of Nanotechnology on the Performance of CMOS Digital Multipliers”, in the Proceedings of International Conference on Circuits, Signals and Systems, IASTED 2004, Clearwater Beach, FL, November 2004.

D. Kudithipudi, R. Kota, **E. John** and Z. P. Tanner, “Power, Area and Delay Performance Comparison of Multipliers for Embedded Systems” in the Proceedings of International Signal Processing Conference, San Jose, California, Oct, 2004.

R. Kuzet, M. Chilikuri, S. Puthenpurayil, H. Foltz and **E. John**, “RF CMOS receiver Front-End Using Reflex Amplifier” Proceedings of IASTED International Conference on Communication Systems and Applications (CSA), Banff, AB, Canada - July 8-10, 2004

S. Petko, D. Kudithipudi and **E. John**, “Memory System Characterization for Multimedia Applications” *International Signal Processing Conference (ISPC)*, Dallas, TX. March 31 – April 3, 2003

M. Wasiewicz, D. Kudithipudi and **E. John** “Low Power Parallel Digital Multipliers using 10 Transistor Adder Circuits” *International Signal Processing Conference (ISPC)*, Dallas, TX. March 31 – April 3, 2003

A. K. Ojha, and **E. John**, “A Paradigm for Testing RISC Processor –Based Complex System–on-Chip (SOC),” Proc. of the IEEE Southeastcon 2003, Ocho Rios, Jamaica, March 2003.

E. John, S. Petko, L. John and J. Law, “Access Time and Energy Tradeoffs for Caches in High Frequency Microprocessors” in *Proceedings of 45th IEEE International Midwest Symposium on Circuits and Systems*, Tulsa, Oklahoma, August, 2002.

S. Petko, D. Kudithipudi and **E. John**, “Cache performance of Video Computation Workloads” *Proceedings of the International Workshop on Digital and Computational Video*, Clearwater, FL, November 2002.

R. Shalem, **E. John** and L. John, "A Novel Low Power Energy Recovery Full Adder Cell" *Proceedings of the Great Lake Symposium on VLSI*, pp. 380-383, 1999

E. John, F. Hudson and L. Kurian "Hybrid Tree: A Scalable Optoelectronic Interconnection Network for Parallel Computing" *Proceedings of the 31st Hawaii International Conference on System Sciences*, Vol. VII, pp. 466-474, January 1998.

L. Kurian, D. Brewer, **E. John**, "Design of a Highly Reconfigurable Interconnect for Array Processors", *Proceedings of the 8th International Conference on VLSI Design*, pp. 321-325, January 1995.

M. Rodriguez and **E. John**, "Design and VLSI Implementation of Arithmetic Circuits", *Proceedings of the ASEE/GSW Conference*, 1999.

H. Saenz and **E. John**, "Design and FPGA Implementation of an 8-bit Processor", pp.228- 233, *Proceedings of the ASEE/GSW Conference*, 1998.

L. Roitberg and **E. John** " Voice Recognition Hardware Interface Using Field Programmable Gate Arrays" pp.230-233, *Proceedings of the ASEE/GSW Conference*, 1997.

E. Lott and **E. John** " Design and Simulation of Solid state Semiconductor Devices" pp.222-225, *Proceedings of the ASEE/GSW Conference*, 1997.

D. Ault, B. Lozano and **E. John** "3-D Graphics Computation using Field Programmable Gate Arrays" pp.226-229, *Proceedings of the ASEE/GSW Conference*, 1997.

E. John and M.B. Das, "Circuit Optimization of Optoelectronic Integrated Lightwave Receivers for Maximum Bandwidth and High-Sensitivity", *Proceedings of the Conference on Emerging Optoelectronic Technologies*, 18-22, July 1994.

E. John, M. B. Das, W-Y. Yang, T.S. Miller, and D. Miller " Fabrication and Performance of a Novel Ultra-Low Capacitance MSM Photodetector for High Speed OEIC Receiver Applications" *Proceedings of the 7th International Conference on InP*

and Related Materials, May 9-13, 1995, Sapporo, Japan

E. John, M. B. Das, Y. W. Yang, and S. M. J. Liu “Extraction of High Frequency Equivalent Network Parameters of HBT’s by Low Frequency Extrapolation of Microwave S-Parameter Data” Proceedings of the 14th *IEEE/ Cornell Conference on High-Speed Semiconductor Devices and Circuits*, pp 141-147, 1993.

C. Areas of Research Interest

Low Power CMOS VLSI Design

VLSI Design

Power Estimation and Optimization

Multimedia and Network Processors

Computer Architecture

Performance Evaluation

Low Power Circuits and Systems

Bi-Modal Biometrics

Workload Characterization of Computer Systems

Low Power Memory Design for Multimedia Applications

Reconfigurable Architectures using Field Programmable Gate Arrays

Design and VLSI Implementation of Arithmetic Circuits

D. Research Support

1. National

Agency: Army Research Office
Title: Energy Efficient RF CMOS Front End Circuits for Wireless Communications
Amount: \$296,500.
Period: 2005 – 2008
Role: Sole-PI

Agency: National Science Foundation
Title: Low Power CMOS Circuits and Systems for Next generation Wireless Information Technology
Amount: \$300,000.
Period: 2002 – 2006
Role: PI

Agency: Air Force Office of Sponsored Research (AFSOR)
Title: Vehicle Engine Health Monitoring
Amount: \$1,000,000 (approx.)
Period: 2004 – 2005
Role: Co-PI (My share approx. \$100,000.)

Agency: Department of Defense
Title: Implementation of UNIX based lab for interactive learning
Amount: \$120,460
Period: 2000
Role: Co-PI

Agency: The National Science Foundation
Title: Design Optimization and Simulation of Optoelectronic Integrated Circuit Photoreceivers
Amount: \$50,000
Period: 1998
Role: Sole-PI

Agency: The National Science Foundation
Title: Low Power Microelectronics
Amount: \$36,268
Period: 1997
Role: Sole-PI

Agency: The National Science Foundation
Title: Applied Electromagnetics Laboratory
Amount: \$25,683
Period: 1997-2000
Role: Sole-PI

2. State

Agency: Advanced technology Program (ATP)/Texas Higher Education
Coordinating Board
Title: High Performance Multimedia Processors
Amount: \$153,000
Period: 1999-2001
Role: Co-PI

Agency: Center of Infrastructure Assurance and Security, UTSA
Title: Bi-Modal Biometrics: Fusion of Finger Print and Voice Print for
Enhanced Biometric Authentication
Amount: \$282,341 (approx.)
Period: 2004-06
Role: PI

Agency: The University of Texas at San Antonio
Title: Low Power CMOS Circuits for 3G Wireless Communications
Amount: \$5,000
Period: 2002
Role: PI

3. Companies

Agency: IBM Corporation
Title: SUR (Shared University Research) Equipment Grant
Amount: \$20,000 (approx.)
Period: 2001
Role: Co-PI

IV. Service

A. Professional Activities:

Current Professional and Scientific Organizations/Societies

Senior Member, Institute of Electrical and Electronics Engineers (IEEE)

Member IEEE Computer Society

Member IEEE Circuits and Systems Society

Meeting/Symposium Organizer/Chairmanship

General Chair, “4th Workshop on Unique Chips and Systems” (UCAS-4), Austin, TX, April, 2008

Program Co-Chair, “The 4th IEEE International Symposium on Embedded Computing”, Niagara Falls, Canada, May 21-23, 2007
(<http://www.cse.ust.hk/~zgu/SEC-07/>)

General Chair, “3rd Workshop on Unique Chips and Systems” (UCAS-3), San Jose, CA, April 8, 2007

General Chair, “2nd Workshop on Unique Chips and Systems” (UCAS-2), Austin, TX, March 19, 2006.
(<http://www.ispass.org/ucas2/>)

General Chair, “Workshop on Unique Chips and Systems”, (UCAS-1), Austin, TX, March 20, 2005.
(<http://ispass.org/ucas1/>)

Program Vice-Chair on Power-aware Computing, The 2005 International Conference on Embedded Systems and Applications **ESA-05**, Las Vegas, Nevada, USA, June 27-30, 2005

Session Chair/Organizer

Technical Program Committee Member, International Workshop on Optimizations for DSP and Embedded Systems (ODES), held in conjunction with IEEE/ACM International Conference on Code Generation and Optimization, San Francisco, March 2005.

Technical Program Committee Member, Workshop on Interaction between Operating System and Computer Architecture (IOSCA 2005), October 8 2005, Austin Texas

Program Committee Member, International Workshop on Optimizations for DSP and Embedded Systems (ODES) –2004

Technical Program committee member; The International Conference on High Performance Computing and Communications

Reviewer for Journals/Conferences

Technical reviewer for IEEE Transactions on VLSI Systems

Technical Reviewer for IEEE Transactions on Circuits and Systems - II

Technical Reviewer for Journal of Solid State Circuits

Technical reviewer for IEEE Transactions on Electron Devices.

Technical Reviewer, Journal of Circuits, Systems, and Computers (JCSC)

Technical Reviewer, International Journal of Computers and Electrical Engineering

Technical reviewer for Journal of Microprocessors and Microsystems

Technical reviewer for IEEE Workshop on Workload Characterization

Technical reviewer for IEEE/ACM *International Symposium on Microarchitecture (Micro)*

Technical reviewer for *International Symposium on High-Performance Computer Architecture (HPCA)*

Technical reviewer for *International Conference on Computer Design (ICCD)*

Technical reviewer for *International Workshop for DSP and Embedded Systems (ODES)*

Technical Reviewer, *Workshop on Optimizations for DSP and Embedded Systems*, San Francisco, March 2005.

Technical reviewer, *Workshop on Unique Chips and Systems (UCAS - 2005)*, Austin, March 2005.

Technical reviewer, *Workshop on Interaction between Operating System and Computer Architecture*, October, 2005, Austin Texas

Review Panels (for grants)

National Science Foundation proposal review panel member - 1997, 2003 & 2004.

B. Committees:

1. Department

- Chair, electrical and computer engineering faculty search committee 2008-09
- Member, electrical and computer engineering faculty search committee 2006, 2007, 2008
- Chair, electrical and computer engineering faculty search committee 2004-2005
- Member Electrical Engineering Faculty Search Committee 2003-2004
- Member electrical engineering department Ph. D. recruitment committee 2002 - 2004
- Member electrical engineering department Graduate Studies Committee 2002 - 2006
- Member electrical engineering department Merit review Committee 2002 - 2005
- Member electrical engineering department curriculum committee 2002 - 2005
- Member electrical engineering department TA selection committee 2004
- Member electrical engineering department curriculum committee 2004
- Member electrical engineering department DFRAC

2. College of Engineering

- Member CFRAC 2008
- Member, college of engineering academic policy and curriculum committee 2004 – 2006
- Member, college of engineering Intellectual Property review committee 2003- 2005
- Member, college of engineering faculty development leaves award committee 2005 – 2007

3. University

- Member UTSA Faculty Senate 2001-present (current term expires in 2009)
- Member UTSA Graduate Council 2001- May 2006
- Member UTSA Assembly 2002 – May 2004
- Chair, Sub-committee on membership, UTSA graduate council 2002-2004
- Member, Agenda Committee UTSA Graduate Council 2002- 2004
- Member faculty senate sub-committee on Nominations, Elections and Procedures
2003-2006

V. OTHER INFORMATION

Founding Faculty Advisor for Eta Kappa Nu Student Chapter at UTSA

Wrote the proposal for the new M. S. in Computer Engineering Program